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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,012	10/31/2003	Eric Adler	21806-00070-US1	8254

30678 7590 08/10/2005

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EXAMINER

POMPEY, RON EVERETT

ART UNIT	PAPER NUMBER
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2812

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/697,012

Applicant(s)

ADLER ET AL.

Examiner

Ron E. Pompey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 20-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 20-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 20 - 27 rejected under 35 U.S.C. 102(b) as being anticipated by Nakagawa et al. (US 5,241,210).

Nakagawa discloses the limitations of:

forming first (59a and 54a fig. 17) and second diffusion regions in a semiconductor substrate; forming a trench (53, fig. 16) structure around said first and second diffusion regions; and forming a contact on said trench structure and said substrate (63a, fig. 17) for controlling current through said diffusion regions; and

forming first (61a, fig.17) and second gates over said first and second diffusion regions with source (56a, and 58a, fig. 17) and drain regions formed in said diffusion on each side of said gate (col. 7, lns. 25-56 and col. 9, lns. 36-48). It is inherent, to one of ordinary skill in the semiconductor device art, that when an applied potential, voltage or current, across a contact in a particular diffusion region; a field is applied at that region

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which will increase or decrease the resistance across that region (see Conner, column 4, lines 7-10, for reference).

3. Claims 20 –27 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al. (US 6,118,152).

Yamaguchi discloses the limitations of:

forming first and second diffusion regions (the fox regions 13a and 13b, fig. 1 define the diffusion regions) in a semiconductor substrate; forming a trench (5, fig. 1) structure around said first and second diffusion regions; and forming a contact on said trench structure (19a and 19b, fig. 1) and said substrate.(18, fig. 1) for controlling current through said diffusion regions; and

forming first (15a, fig.1) and second (15b, fig.1) gates over said first and second diffusion regions with source (9, 12a and 12b, fig. 1) and drain regions formed in said diffusion on each side of said gate (col. 3, ln. 25 - col. 5, ln. 4). It is inherent, to one of ordinary skill in the semiconductor device art, that when an applied potential, voltage or current, across a contact in a particular diffusion region; a field is applied at that region which will increase or decrease the resistance across that region (see Conner, column 4, lines 7-10, ^{supporting} for reference)

Response to Arguments

4. Applicant's arguments filed 4-15-05, pertaining to claims 20-27, have been fully considered but they are not persuasive. The applicant argues that "...the "control electrode" disclosed by Nakagawa is *not* formed on the "trench structure,"...". However, Nakagawa discloses, in column 7, lines 26-32, that oxide 53/53a, see figures 6/17

respectively, forms a groove/trench and figure 17 shows an electrode clearly on section 64a which is filled into groove/trench 53/53a. Therefore the control electrodes are on the trench structure and read on the claims.

Also, the applicant argues that "...the "control electrode" (i.e., gate electrodes 15a, 15b) disclosed by Yamaguchi et al are *not* formed on the "trench structure," ...". However, Yamaguchi discloses, in column 3, lines 42-48, that oxide 6 forms on the inside walls of trench 5 and control electrodes 19a/19b are clearly on sections 7 which are filled into trench 5, see figure 1 and column 4, lines 24-53. Therefore the control electrodes are on the trench structures and read on the claims. Note that in the above rejection the control electrode on the trench are electrodes 19a/19b not the gate electrodes 15a/15b as cited in applicant's response/arguments.

Conclusion

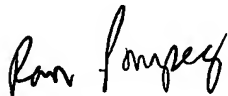
5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on compressed.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Ron Pompey
AU:2812
July 28,2005


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER